

CHARACTERISTICS OF A NONVOLATILE SRAM MEMORY CELL UTILIZING A FERROELECTRIC TRANSISTOR

Cody Mitchell¹, Crystal Laws¹, Todd C. MacLeod², Fat D. Ho¹

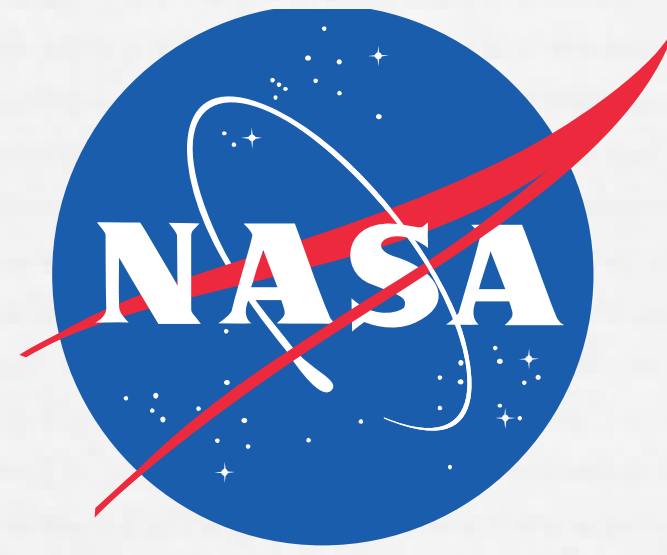
¹The University of Alabama in Huntsville, Department of Electrical and Computer Engineering,
Huntsville, Alabama 35899, USA

²National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville,
Alabama 35812, USA

Abstract

The SRAM cell circuit is a standard for volatile data storage. When utilizing one or more ferroelectric transistors, the hysteresis characteristics give unique properties to the SRAM circuit, providing for investigation into the development of a nonvolatile memory cell. This paper discusses various formations of the SRAM circuit, using ferroelectric transistors, n-channel and p-channel MOSFETs, and resistive loads. With varied source and supply voltages, the effects on the timing and retention characteristics are investigated, including retention times of up to 24 hours.

Keywords: SRAM, nonvolatile, ferroelectric

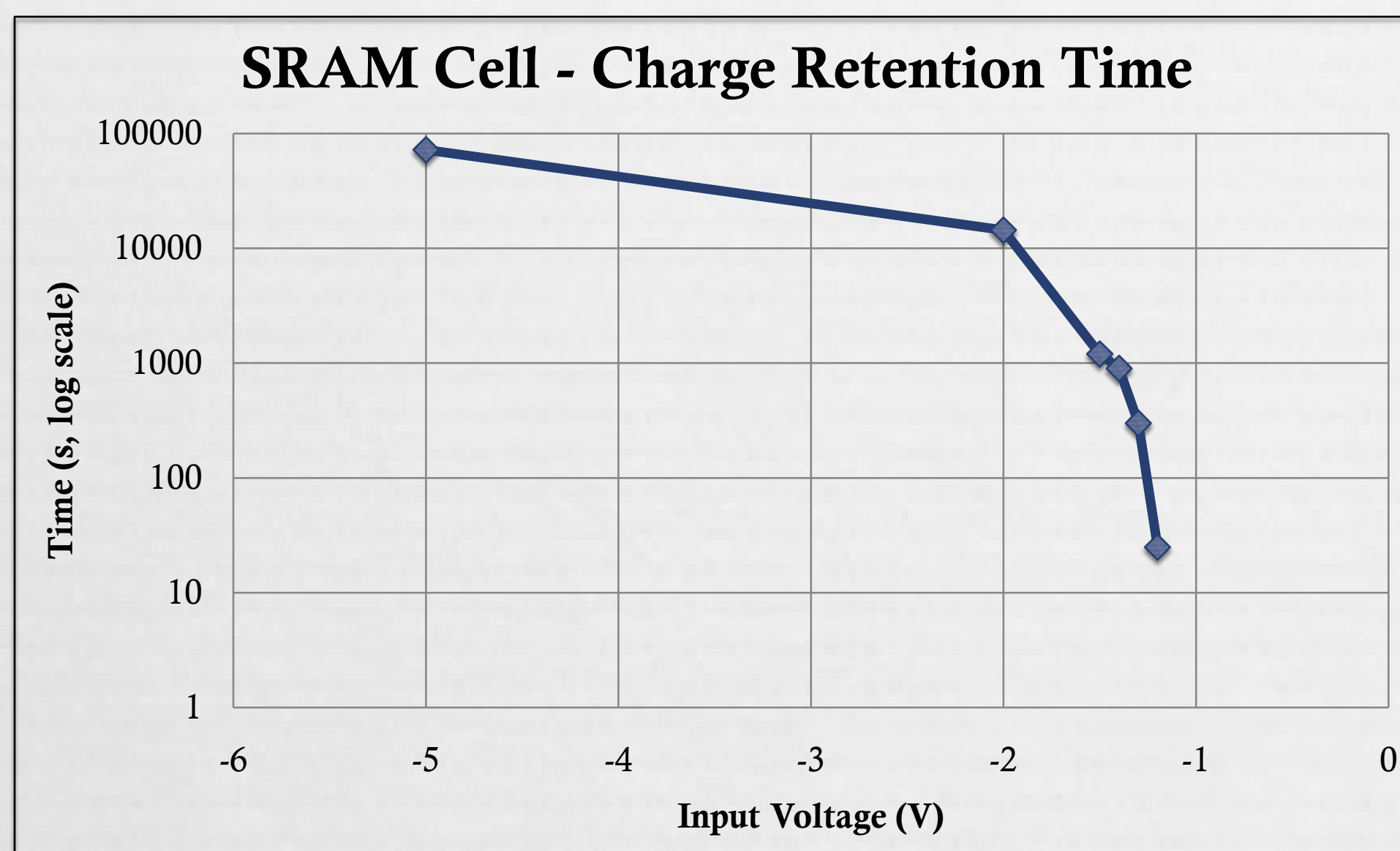


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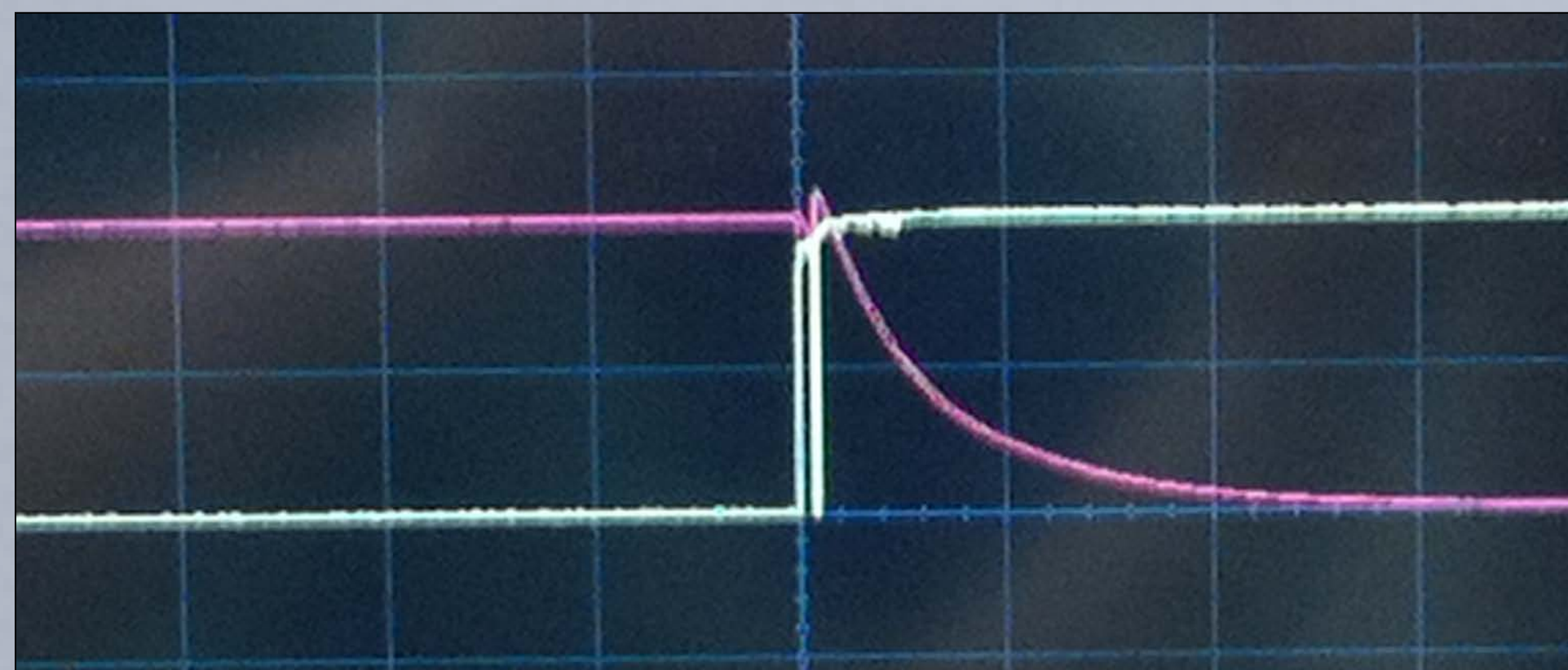
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¹University of Alabama In Huntsville, Department of Electrical and Computer Engineering, Huntsville, AL 35899, U.S.A

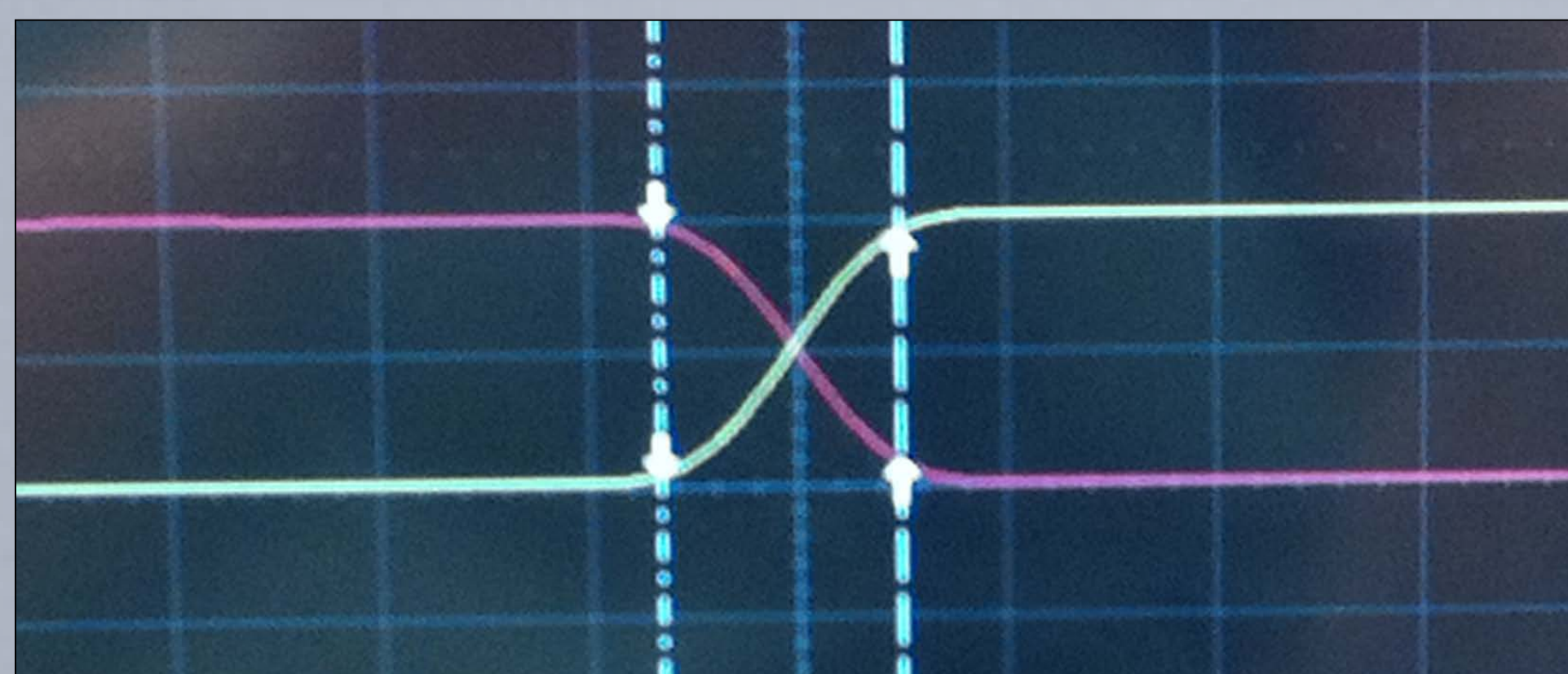
²National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville, AL 35812, U.S.A



Charge retention tests were conducted by applying and removing a charge at Node 1 of the SRAM circuit, removing V_{DD} , and then reapplying V_{DD} to see what value was shown at Node 2. A critical point was discovered around -1.2 V that influenced whether a charge was truly retained for a substantial number of seconds. Tests showed that a more negative input voltage resulted in a longer retention period, with an input voltage of -5 V lasting at least 20 hours.



In these oscilloscope readings from experimental testing of the SRAM circuit, it is shown that placing a single FeFET in the SRAM circuit produces very different results depending on which side of the circuit contains the FeFET. Placing the FeFET on the left (Node 1) side of the circuit results in a slow decrease of the Node 2 voltage (shown above). The image below shows that placing the FeFET on the right (Node 2) side of the circuit results in symmetric transitions of the voltages at both Nodes 1 and 2.



Introduction

The SRAM cell is a standard circuit for volatile memory storage. When one more ferroelectric field-effect transistors (FeFETs) are introduced into the circuit, it is possible to develop a nonvolatile memory cell.

Ferroelectric-based memory cells offer benefits over existing nonvolatile memories, such as FLASH. While FLASH may offer lower cost and better storage densities, ferroelectric memory offers the potential for faster performance, lower power consumption and voltage requirements, and more write cycles.

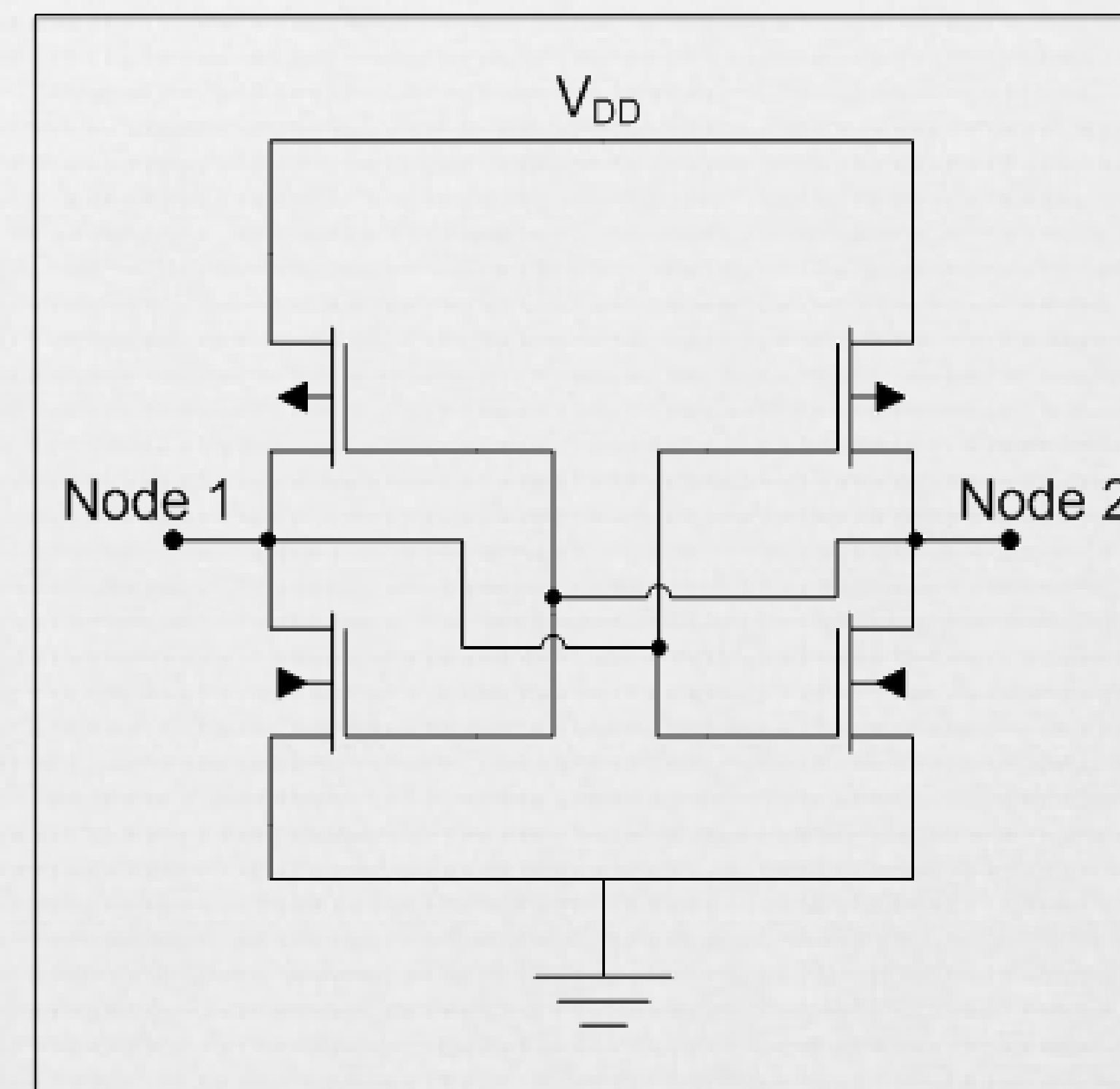
The focus of this series of experiments was to investigate the performance of a ferroelectric-based SRAM cell, specifically the response time of Node 2 with respect to an applied or removed voltage at Node 1, and the overall capability of the circuit to perform as a nonvolatile memory cell.

SRAM Circuit Configuration

An SRAM circuit was constructed in various configurations utilizing traditional MOSFETs and FeFETs as driver transistors. The FeFETs were provided by Joe Evans of Radiant Technologies, Inc. in Albuquerque, New Mexico. The FeFETs were NMOS transistors and featured a channel width of 400 μm and a channel length of 4 μm . PMOS FeFETs were not available for SRAM testing.

Some of the key configuration differences investigated were:

- the impact of placing a single FeFET into the SRAM circuit on the Node 1 side of the circuit, with a traditional n-channel MOSFET at Node 2
- the impact of placing a single FeFET into the SRAM circuit on the Node 2 side of the circuit, with a traditional n-channel MOSFET at Node 1
- the impact of replacing both n-channel MOSFETs with FeFETs
- the usage of PMOS transistors as loads in comparison with resistors
- the effect of different load resistor values



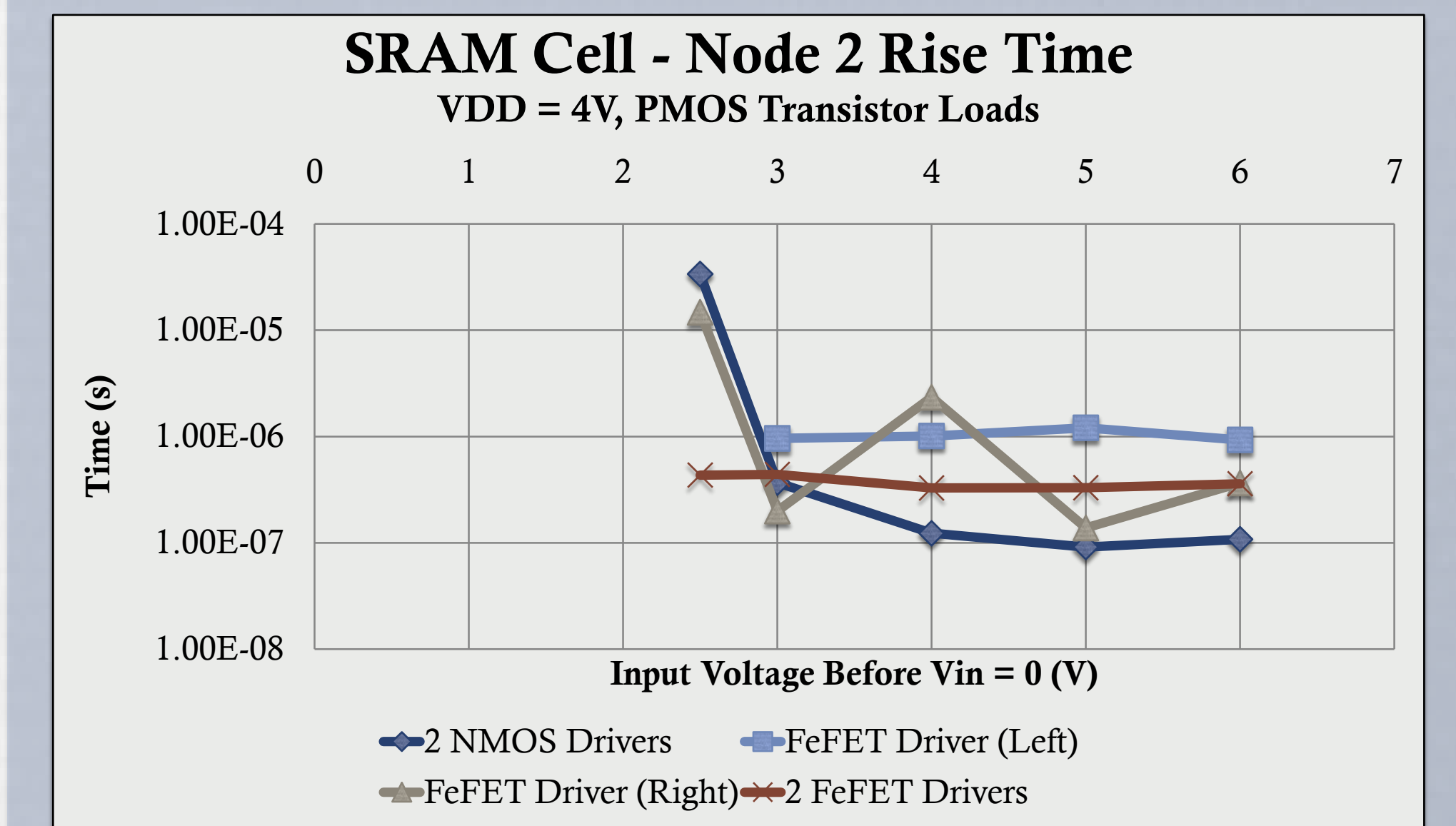
SRAM Circuit

Summary

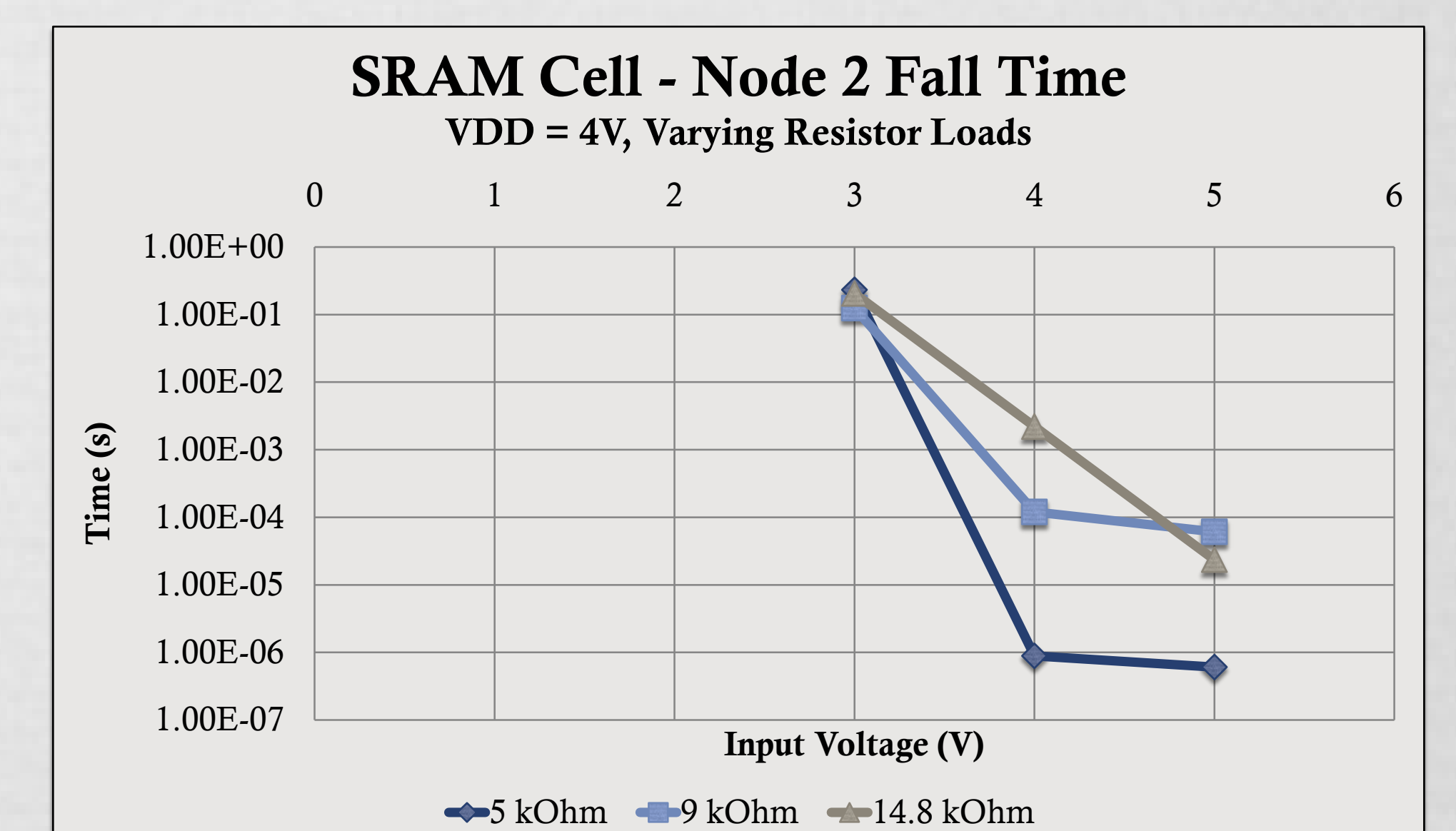
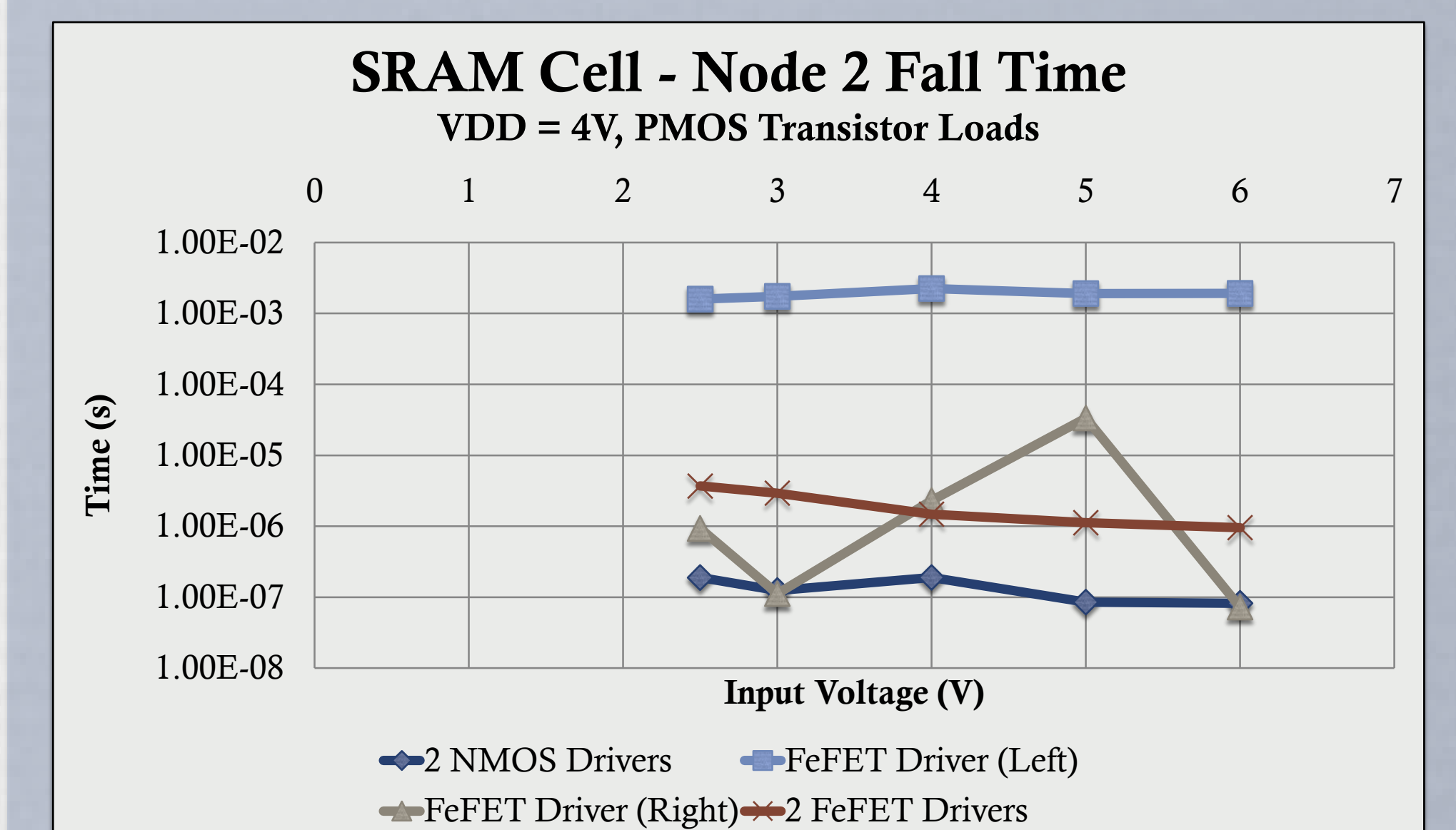
When utilizing one or more ferroelectric transistors, the hysteresis characteristics give unique properties to the SRAM circuit, providing for investigation into the development of a nonvolatile memory cell. Tests proved that it was possible for the circuit to retain a stored value for nearly one day with supply power removed. In addition to retention, the timing characteristics with ferroelectric transistors at both Nodes 1 and 2 show similar results to those of the traditional n-channel MOSFETs. Also, the SRAM cell results in quicker response times for lower load resistances, with 5 kOhm being the optimal case. Overall, the SRAM cell using ferroelectric transistors performs rather well as a nonvolatile memory cell, even though the circuit was not optimized for memory retention applications.

References:

1. Y. Tsividis, Operation and Modeling of The MOS Transistor, 2nd Ed., Oxford, New York, 1999.
2. T. A. Phillips, M. Bailey, and F. D. Ho, A Novel Metal-Ferroelectric-Semiconductor Field-Effect Transistor Memory Cell Design. *Integrated Ferroelectrics* 67, 229-234 (2004).
3. Sanyo, "Very High-Speed Switch, Analog Switch Applications," 2SK669 datasheet, April 1999.
4. Zetex Semiconductors, "P-Channel Enhancement Mode Vertical DMOS FET," ZVP4105A datasheet, March 1994.



The fall and rise times of Node 2 of the SRAM cell suggest that using two FeFETs in an SRAM circuit will provide better performance than using only a single FeFET. This is apparent when looking at the fall time of the circuit, where it is shown that including only a single FeFET on the left side of the circuit is much slower than the other configurations.



When replacing the PMOS loads with resistors, lower resistances provide quicker response times at Node 2 of the SRAM circuit.